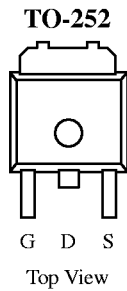


N-Channel Enhancement-Mode MOSFETs, Logic Level

Product Summary

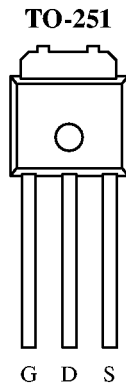
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.022 @ $V_{GS} = 10$ V	34
	0.025 @ $V_{GS} = 4.5$ V	34

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs

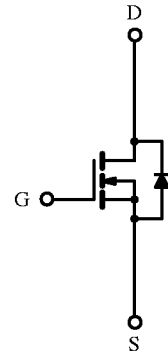


Order Number:
SUD40N06-25L

Drain Connected to Tab



Order Number:
SUU40N06-25L



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^b	I_D	$T_C = 25^\circ\text{C}$	34
		$T_C = 100^\circ\text{C}$	24
Pulsed Drain Current	I_{DM}	100	A
Continuous Source Current (Diode Conduction)	I_S	34	
Avalanche Current	I_{AR}	34	
Repetitive Avalanche Energy (Duty Cycle $\leq 1\%$)	E_{AR}	$L = 0.1$ mH	58
Maximum Power Dissipation		$T_C = 25^\circ\text{C}$	75
		$T_A = 25^\circ\text{C}$	1.4 ^a , 2.5 ^b
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R_{thJA}	Free Air, FR4 Board Mount	60
		Free Air, Vertical Mount	110
Maximum Junction-to-Case	R_{thJC}	2.0	$^\circ\text{C/W}$

Notes:

- a. Free air, vertical mount.
- b. Surface mounted on 1" x 1" FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70264. A SPICE Model data sheet is available for this product (FaxBack document #70567).

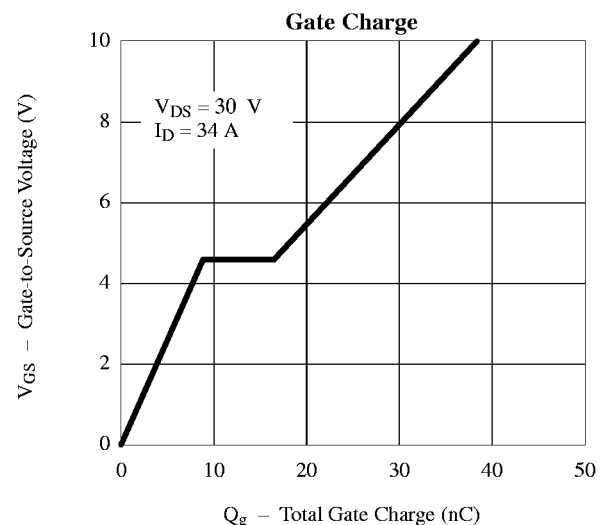
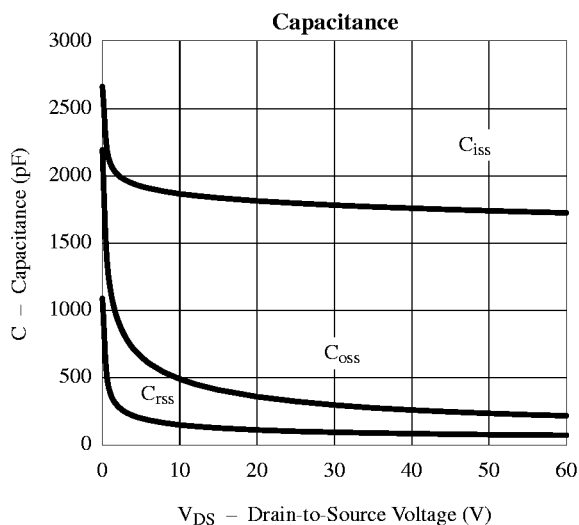
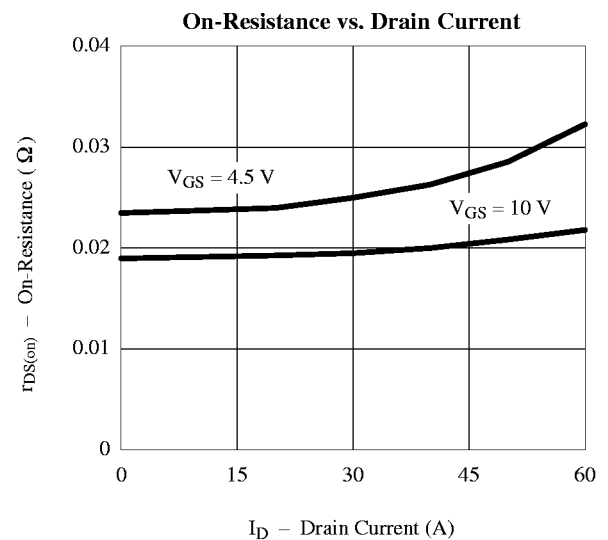
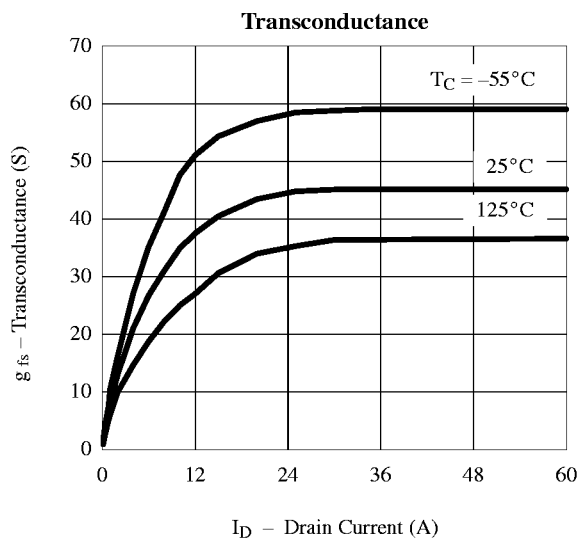
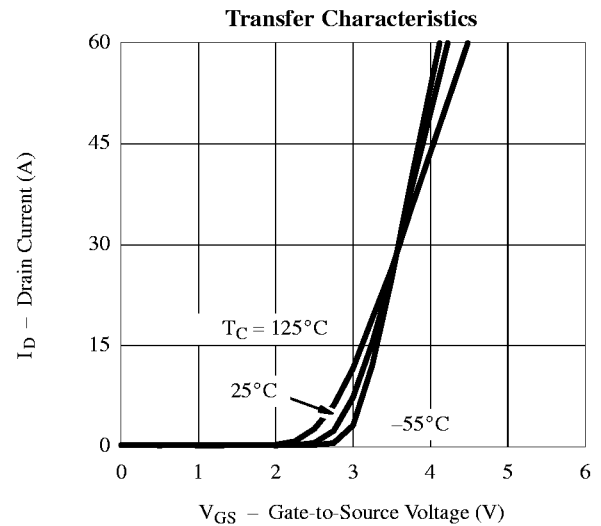
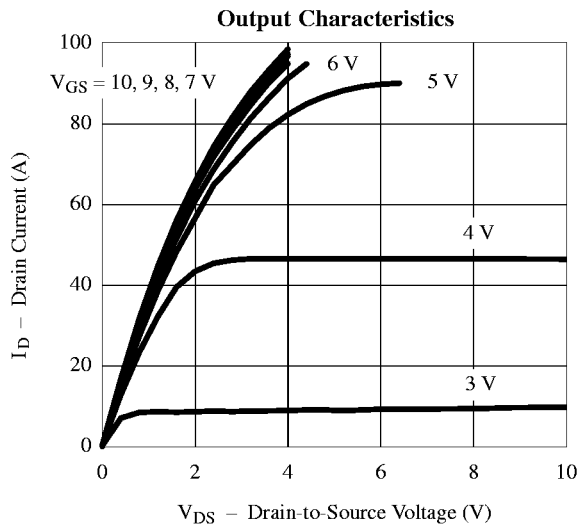
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			50	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$			150	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	34			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$			0.022	Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125^\circ\text{C}$			0.043	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 175^\circ\text{C}$			0.053	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$			0.025	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$				S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		1800		pF
Output Capacitance	C_{oss}			350		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		40	60	nC
Gate-Source Charge ^c	Q_{gs}			9		
Gate-Drain Charge ^c	Q_{gd}			10		
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.9\ \Omega$ $I_D \approx 34\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\ \Omega$		10	20	ns
Rise Time ^c	t_r			9	20	
Turn-Off Delay Time ^c	$t_{d(off)}$			28	50	
Fall Time ^c	t_f			7	15	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$)						
Pulsed Current	I_{SM}				34	A
Diode Forward Voltage	V_{SD}	$I_F = 34\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 34\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		48	100	ns

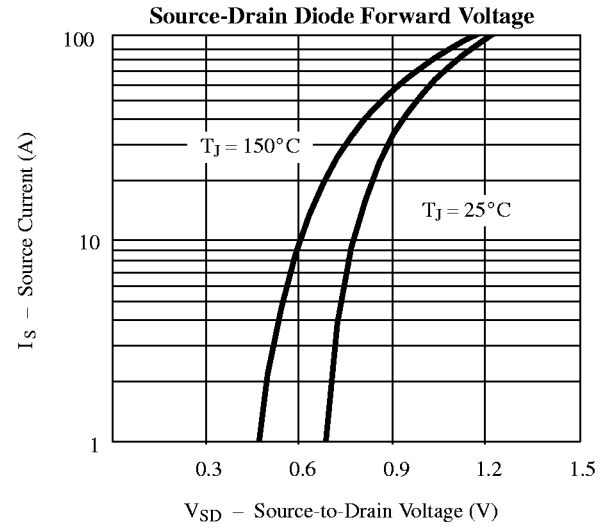
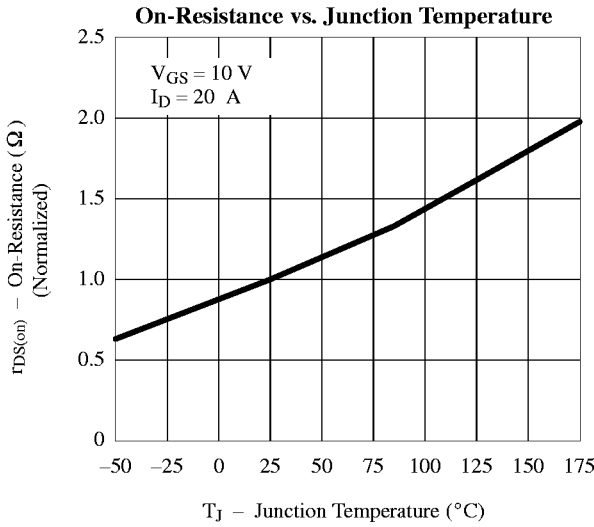
Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)



Thermal Ratings

